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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,772	08/01/2005	Christopher Rodd Speirs	CH02 0021 US	4888
65913	7550	10/27/2009		
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER ABDIN, SHAHEDA A	
			ART UNIT	PAPER NUMBER
			2629	
			NOTIFICATION DATE	DELIVERY MODE
			10/27/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

### Office Action Summary

**Application No.**

10/518,772

**Applicant(s)**

SPEIRS ET AL.

**Examiner**

SHAHEDA A. ABDIN

**Art Unit**

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 August 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 August 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. The amendment filed on 06/23/2009 has been entered and considered by Examiner.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 4, 8, 13-14, 9 and 12 are rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The new limitation “**prevent the n outputs**” has been recited in the claims 4, 8, 13-14, 9 and 12. There is no explicit description contained in the specification for this new limitation.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohta. (US. Patent No: 20010033278 A1).

(1) Regarding claim 9:

Ohta teaches the row drive circuit (3) for controlling n rows of a display device (1) that is operable in a partial mode ([0026-0027]), the row drive circuit (3) comprising :

a shift register (32) having n stages (e.g. 32g, 32d) and n outputs (output from 32g and 32d) and a logic function (i.e. Flip-flop 37c ) connected in front of each of the n outputs of the shift register (see the illustration in Fig. 3, the row driver circuit (3) is including a shift register 32 and logic function e.g. Flip-flop 37 is connected in front of each of the row output e.g. OG1, OG2.....), the logic function deactivate n outputs (i.e. respective row output for non-display portion and display portion) of the shift register

in dependence on the partial mode responsive to a first control signal (i.e. signal from GCNT1/2, see Fig. 2) (also see [0028, 0032-0035]) by preventing (stop the voltage signal for **unscanned area, [0058] and [0060]**) the n outputs of the shift register from driving the n rows (i.e. rows corresponding to the non display portion) of the display device (1) ( note the signals are outputted from the shift register (i.e. 32) in accordance with the logic function (i.e. 37) to respective scanning lines and has a partial display function for a non-image area and an image display area that means the logic function (37) configured to prevent the shift register's output not to be displayed in respective scanning lines in the partial mode in the row drive circuit [0013] and Fig. 2) (see the illustration in Fig. 3, also see [0033-0035]).

(2) Regarding claim 12:

Ohta teaches a method (in Fig. 1-6) of realizing a partial mode (display divided in to non-display portion and display portion) of a display device, the display device controlled by a circuit arrangement that includes a row drive circuit (i.e. 3) for driving n rows (i.e. OG1-OGI) and a column drive circuit (2) for supplying column voltages to m columns [0026-0028], the method comprising:

sequentially (line by line) providing an enable signal (GSP) to each row from 1 to n (OG1-OGI) (see Fig. 2) ([0032-0033]);

supplying (supplying through the column driver 2) the column voltages to the m columns for displaying corresponding picture data ([0031]). ,

deactivating all row outputs (deactivating all row outputs in non display portion) of a first row (row for the non display portion) of the row drive circuit (3) in response to a first control signal (GCNT1/2) indicating that the first row is not to be displayed in the partial mode of the display device (see Fig. 2, [0017], [0051]), and by preventing the row outputs of the first row from driving the display device, (stop the voltage signal for unscanned area, [0058] and [0060])) and

activating all row outputs (activating all row outputs in display portion) of a second row, in response to the enable signal (GSP) and the first control signal (GCNT1/2), indicating that the second row is to be displayed in the partial mode ([0060], see Fig. 2).

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8, 10-11 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta.

(1) Regarding claim1:

Ohta in Fig. 2 teaches a circuit arrangement for controlling a display device (1) which can be operated in a partial mode (display divided in to non-display portion and display portion) [0026], the circuit arrangement comprising:

a row drive circuit (3) for driving n rows (OG1-OGI) of the display device (1) sequentially (line by line) from 1 to n, the row drive circuit responsive to a row enable signal (i.e. GSP) that is provided to each row from 1 to n ([0028]); and

a column drive circuit (i.e. 2) for driving m columns (data signal lines) of the display device (i.e. 1), by supplying column voltages to the m columns [003], the column voltages corresponding to picture data (image data) to be displayed as pixels of the controlled row [0027-0028], characterized in that a logic function (logic function from control IC 4, note that controller 4 is interpreted as a control logic which function is interpreting as a logic function; the display portion and non display portions are set in advanced by the control IC 4, [0047]) is included in the row drive circuit (3) in front of at least one row output (note that the gate driver 3 including a control logic section 31 which is corresponding to controller IC4 is placed in front of row output) ([0033-0034]), the logic function configured and arranged to respond to a first control signal (i.e. GCNT1/2 corresponding to display scanning signal or display 'ON' signal), indicative of whether or not the partial mode is to be implemented (apply) [0036], is supplied.

Note that Ohta teaches all of the limitation as recited in claim, but Ohta does not explicitly discloses the limitations "first control signal achieving a deactivation/activation of by preventing the at least one row output from driving the row in response to the

row enable signal (GSP) in dependence on the partial mode", such limitation are merely would have been obvious in the system of "Ohta". The limitations do not define a patentably distinct invention over that in "Ohta" since the invention as a whole and "Ohta" are directed to first control signal (GCNT1/2) achieving a deactivation/activation (i.e. deactivate row outputs to the Non-display area while activating the row outputs to the display area) of by preventing the at least one row output from driving the row in response to the row enable signal (GSP) in dependence on the partial mode ([0038-0039]). Therefore, "Ohta" would have been a matter of obvious choice to one of ordinary skill in the art to acquire the limitations "first control signal achieving a deactivation/activation of **by preventing the at least one row output from driving the row** in response to the row enable signal (GSP) in dependence on the partial mode". In this configuration the system would provide an optimum output to the display device, thereby reducing power consumption in the scanning signal line driving section (Ohta, [0017]).

(2) Regarding claim 2:

Ohta teaches the logic function (e.g. 37b, 37d) is connected in front of each row output (i.e. in front of row lines e.g. OG1-OGI) (see Fig. 3).

(3) Regarding claim 3:

Ohta teaches the logic function is realized as an AND gate (AND circuit 37a) [0044].

(4) Regarding claim 4:



Ohta teaches the row drive circuit (3) comprises a shift register (3) which has n stages (e.g. 32g, 32d) and n outputs (output from 32g and 32d), and in that a second control signal (i.e. control signal from GCK) can be supplied to the shift register (32) at an input thereof for controlling the consecutive rows 1 to n (i.e. gate lines OG1-OGI), which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal and wherein the logic function (37) is connected between the n outputs of the shift register (i.e. output from the shift register 32) and the n rows (e.g. OG1, OG2) of the display, the logic function configured to prevent ((stop the voltage signal for **unscanned area, [0058] and [0060]**))) the n outputs of the shift register from driving the n rows of the display responsive to the first control signal (note the signals are outputted from the shift register (i.e. 32) in accordance with the logic function (i.e. 37) to respective scanning lines and has a partial display function for a non-image area and an image display area that means the logic function (37) configured to prevent the shift register's output not to be displayed in respective scanning lines in the partial mode in the row drive circuit [0013] and Fig. 2) (see the illustration in Fig. 3, also see [0033-0035]).

(5) Regarding claim 5:

Ohta teaches the first control signal (GCNT1/2 corresponding to display scanning signal) is capable of switching off (that is changing "ON" to "OFF") all n row outputs by

means of the logic function during control of a line that is not to be displayed in the partial mode (i.e. non display portion e.g. 1b, 1c) ([0030-0034], and [0051]).

(6) Regarding claim 6:

Ohta teaches that control logic (IC4) in the column drive circuit generates the first control signal (signal from GCNT1/2 corresponding to scan "ON" signal) in dependence on the partial mode and supplies the first control signal to the row drive circuit ([0030-0034], and [0051]).

(7) Regarding claim 7:

Ohta teaches the column drive circuit (2) supplies no column voltages to the m columns (i.e. deactivate the operation of the source driver) in a case of a line that is not to be displayed ([0049]).

(8) Regarding claim 8:

Ohta teaches the frequency of the clock signal (GCK) can be increased in a case of one or several consecutive rows (i.e. non display portion 1a, 1b) that is or are not to be displayed ([0065]).

(9) Regarding claim 10:

Ohta teaches that a display device (1) comprising a circuit arrangement (see the illustration in Fig. 1-4).

(10) Regarding claim 11:

An electronic appliance (i.e. LCD in Fig. 2) comprising a display device (1) ([0027])

(11) Regarding claim 13:

Ohta teaches wherein each of the stages includes a flip-flop (e.g. 32) (see the illustration in Fig. 3).

(12) Regarding claim 14:

Ohta discloses the first control signal (signal from GCNT1/2 corresponding to "ON" signal) overrides (make ineffective) the second control signal (i.e. signal from GCK) ([0036]) (note that the second control signal i.e. GCK is applied to the output lines (i.e. gate lines); the shift register control block 32 signaled by the gate start pulse from the control logic section 31, and output the scanning signal for outputting for outputting the ON signal. Thus, the first control signal override the second control signal from GCK).

### ***Response to Arguments***

8. Applicant's arguments, with respect to claim 1-14 have been considered but are not persuasive.

Applicant argues that "the reference of Ohta does not teach deactivating the row outputs of a row drive circuit by preventing the row outputs from driving the display. Instead the driver circuit of Ohta simultaneously applied drive signal to the respective scan lines in the non display portions".

Examiner disagree Applicant's point of view. Note that the claim limitations

" **preventing the row outputs**" are broadly recited in the claims. The claim language does not exclude the limitations " **simultaneously applied drive signal to the respective scan lines in the non display portions**". Moreover, Ohta in paragraph [0060] discloses that the scanning signal lines which correspond to the non-display portions making up the unscanned area (logic function prevent or stop the voltage signal for **unscanned area, [0058] and [0060]]**) are divided into a first line group and a second line group of, the scanning can be realized, for example, by controlling the circuit as shown in FIG. 3 according to the first line group and the second line group of, for example, odd line numbers and even line numbers, respectively.

### Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing

date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### **Inquiry**

10. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Shaheda Abdin** whose telephone number is (571) 270-1673.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard HJerpe** could be reached at (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pari-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Richard Hjerpe/

Supervisory Patent Examiner, Art Unit 2629

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